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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	TODD A. MERRITT NICHOLAS VANHEEL	Group Art Unit:	2133
		Examiner:	JOSEPH D. TORRES
Serial No.:	10/712,150	Conf. No.:	8235
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For:	COMPRESSION CIRCUIT FOR TESTING MEMORY DEVICE	CUSTOMER NO.:	23720

APPEAL BRIEF

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8	
DATE OF DEPOSIT:	May 9, 2006
I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as "FIRST CLASS MAIL" addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
Nancy Nolan Signature	

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On February 6, 2006, Appellants filed a Notice of Appeal in response to a Final Office Action dated October 5, 2005, issued in connection with the above-identified application. In support of the appeal, Appellants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences.

Since the Notice of Appeal for the present invention was received and stamped by the USPTO Mailroom on February 9, 2006, the two-month date for filing this Appeal Brief is April 9, 2006. An extension of one month is hereby requested, therefore, the due date for filing the Appeal Brief is May 9, 2006 (with a one month extension). Since this Appeal Brief is being filed on May 9, 2006, it is timely filed with a one-month extension.

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Since there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

The Commissioner is authorized to deduct a fee of $620 ($500.00 filing fee and $120.00 for a one-month extension) from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2008.001982. No other fee is believed to be due in connection with the filing of this document. However, should any fee under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to this document, the Commissioner is hereby authorized to deduct said fee from **Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2008.001982**.

I. REAL PARTY IN INTEREST

The present application is owned by Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF CLAIMS

Claims 31, 32 and 38-54 remain pending in this application.

IV. STATUS OF AMENDMENTS

After the Final Rejection, no other amendments were made to any other claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In general, the present invention is directed to the testing of memory devices, and more particularly to the testing of memory devices using a compression circuit. There are two independent claims at issue in the current appeal: claims 31 and 38.

Independent claim 31 is generally directed to a method for testing a memory device having a plurality of data lines. The method comprises latching data present on at least a subset of the plurality of data lines based upon an enable signal, wherein at least two of said plurality of data lines are latched from two respective memory portions. The method further comprises masking the latched data from said at least two of said plurality of data lines and compressing the masked data to determine if the masked data matches a predetermined pattern using a compressing circuit. Finally, the method of claim 31 includes providing at least a pass signal if the masked data matches the predetermined pattern. By way of example only, at least portions of the invention are described at p.11-15 and 19-20; Figures 3-5B and 7-8.

Independent claim 38 is generally directed to an apparatus for testing a memory device having a plurality of data lines. The apparatus comprises means for latching data present on at least a subset of the plurality of data lines based upon an enable signal, wherein at least two of said plurality of data lines are latched from two respective memory portions. The method further comprises means for masking the latched data from said at least two of said plurality of data lines and means for compressing the masked data to determine if the data matches a predetermined pattern using a compressing circuit. Finally, the method of claim 31 includes means for providing at

least a pass signal if the data matches the predetermined pattern. By way of example only, at least portions of the invention are described at p.11-15 and 19-20; Figures 3-5B and 7-8.

For example, referring to Figure 3, embodiments of the present invention describe and claim an embedded device 100 that includes a processor 105 and four memory device cores 110. A data latch 115 is coupled to the processor 105 and the memory device cores 110 for holding data read from the memory device cores 110. The memory device cores 110 each have data input/output lines (DQ lines) 120 that are connected in parallel to the data latch 115. The processor 105 may only access one of the memory device cores 110 at any given time. Accordingly, the DQ lines 120 of the other non-enabled memory device cores 110 will be in a tristate condition, allowing the enabled memory device core 110 to drive its DQ lines 120 to the data latch 115. The DQ lines 120 of the memory device cores 110 are also coupled to a compression circuit 125. The compression circuit 125 is coupled to output pads 130 that may be accessed externally. See Appellants specification at page 11, ll. 10-21.

Although the compression circuit 125 is described in the context of an embedded device 100 including a plurality of memory device cores 110, its application is not so limited. It is contemplated that the concepts described herein may be applied to other applications, such as stand-alone commodity memory devices (not shown). See Appellants specification at page 12, ll. 1-4.

The compression circuit 125 receives and compresses a plurality of the DQ lines 120 and provides an output indicating whether the data present on the DQ lines 120 that

was read from one of the memory device cores 110 matches the pattern that was written into that memory device core 110. Unlike the compression circuit 10 of Figure 1, the compression circuit 125 compresses data on the DQ lines 120 leaving the memory device cores 110, as opposed to the I/O lines (not shown) within the memory device cores 110. This allows the compression circuit 125 to be shared by the memory device cores 110, thus permitting each of the memory device cores 110 to be tested without duplicating compression logic. Also, because the compression circuit 125 is separate from the memory device cores 110, changes in the design or density of the memory device cores 110 do not require re-design or modification of the compression circuit 125. See Appellants specification at page 12, ll. 5-15.

In the illustrated embodiment, each memory device core 110 has 64 DQ lines 120 and four output pads 130. Accordingly, the compression circuit 125 is adapted to perform a 16 to 1 compression to populate the output pads 130. Other compression ratios are contemplated depending on factors such as the number of DQ lines 120 exiting each memory device core 110 and the number of output pads 130 available on the embedded device 100. See Appellants specification at page 12, ll. 16-20.

The compression circuit 125 also includes input circuits 212, 214 adapted to selectively mask out individual DQ lines 120. See Appellants specification at page 13, ll. 14-16.

Masking selective DQ lines 120 has several advantages. First, by masking selected DQ lines 120, smaller subsets of the DQ lines 120 can be compressed and tested to determine the specific location of a faulted cell (not shown) within one of the memory

device cores 110. This allows a faulted bit (not shown) to be located without a time consuming bit-by-bit check. See Appellants specification at page 15, ll. 1-4.

Another advantage to masking selective DQ lines 120 involves setting the compression ratio of the compression circuit 125. For example, the compression circuit 125 could receive 16 DQ lines 120 (*i.e.*, compression ratio of 16 to 1). Certain DQ lines 120 could be masked to reduce the compression ratio of the compression circuit 125 to, for example 8 to 1 or 4 to 1. See Appellants specification at page 15, ll. 5-8.

In light of this disclosure, the selective masking technique described above may be scaled to any desired compression ratio, depending on the specific size and nature of the embedded device 100 and its associated memory device cores 110. See Appellants specification at page 15, ll. 15-18.

It is contemplated that the input circuit 212, 214 may be modified to allow a single enable line 225 to mask a plurality of the DQ lines 120, depending on the specific implementation and the desired level of control. See Appellants specification at page 18, ll. 3-6.

Figure 7 illustrates an alternative embodiment of an embedded device 450. In this embodiment, the compression circuit 125 is coupled to the output of the data latch 115. Coupling the compression circuit 125 in this manner accomplishes the latching function of the latch 305 in the input circuits 300,302 of Figures 5A and 5B without requiring additional logic for the latch 305. The compression circuit 125 of Figure 7 may include the enabling function for masking individual DQ lines 120 as described above in reference to Figure 4. See Appellants specification at page 19, ll. 15-20.

Figure 8 illustrates the coupling arrangement between the DQ lines 120 of one of the memory device cores 110 and the compression circuit 125. To prevent electrical shorts and capacitive coupling to disguise faults within the memory device core 110, DQ lines 500 of a first topology type (*e.g.*, Type A) are interleaved with DQ lines 510 of a second topology type (*e.g.*, Type B). It is unlikely that two Type A DQ lines 500 could short together without also shorting to a Type B DQ line 510. The short between the Type A DQ line 500 and the Type B DQ line 510 can be detected by the compression circuit 125. Also, because the Type A DQ lines 500 have a different topology than the Type B DQ lines 510, they will not be concurrently transitioning to the same logic level, and as such, a capacitive coupling error is unlikely. See Appellants specification at page 19, l. 20- page 20, l. 7.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 31, 32 and 38-54 are indefinite under 35 U.S.C. 112, second paragraph.

2. Whether claims 31, 32 and 38-54 are unpatentable under 35 U.S.C. 102(e) over U.S. Patent 6,311,299 ***(Bunker)***.

3. Whether claims 31, 32 and 38-54 are unpatentable under 35 U.S.C. 102(f) over U.S. Patent 6,311,299 ***(Bunker)***.

VII. ARGUMENT

Appellants respectfully submit that the Examiner erred in rejecting that claims 31, 32 and 38-54. Therefore, Appellants respectfully request that the rejection of claims 31, 32 and 38-54 under the 35 U.S.C. §102(e) be reversed.

A. Claims 31, 32 and 38-54 Are not indefinite

In the Final Office Action dated October 5, 2005, the Examiner rejected claims 31, 32 and 38-54 under 35 U.S.C. 112, second paragraph, asserting indefiniteness. Appellants respectfully traverse this rejection. Appellants respectfully assert that the term "at least two of said plurality of data lines are latched from respective memory portions" is readily understood by those skilled in the art as having respective relationship with respective memory portions. The "plurality of data lines" are part of the memory device and contrary to the Examiner's assertion, there is no need to specifically recite that different portion of the memory having their own data lines to be definite. It would be clear to those skilled in the art having benefit of the present disclosure that at least two of the plurality of data lines are latched from two respective memory portions, without having to recite that each memory portion has its own data lines. Further, there is no evidence or persuasive arguments to support Examiner's contention that the term "respective" requires a prior indication of memory elements being related to some other element. *See*, page 2 of the Final Office Action dated October 5, 2005. In the context of the claim language is would be clear and definite to those skilled in the art that two of the data lines are latched from two respective memory portion. In the ordinary use of this term, it would be clear to those skilled in the art that this term refers to one of the data lines being latched from one memory portion and the other data line being latched from another memory portion, which is clearly provided by the phrase "wherein at least two of

said plurality of data lines are latched from two respective memory portions" in claims 31 and 38. Accordingly all of the term of claims 31 and 38 are definite and meet the entire requirement of 35 U.S.C. 112, second paragraph. Hence, the Examiner erred in maintaining this rejection and accordingly, claims 31 and 38 are allowable.

B. Claims 31, 32 and 38-54 Are Allowable Over *Bunker*

1. Legal Standards

As the Board well knows, an anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). To the extent the Examiner relies on principles of inherency in making the anticipation rejections in the Office Action, inherency requires that the asserted proposition necessarily flow from the disclosure. *In re Oelrich*, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981); *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1463-64 (Bd. Pat. App. & Int. 1990); *Ex parte Skinner*, 2 U.S.P.Q.2d 1788, 1789 (Bd. Pat. App. & Int. 1987); *In re King*, 231 U.S.P.Q. 136, 138 (Fed. Cir. 1986). It is not enough that a reference could have, should have, or would have been used as the claimed invention. "The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Oelrich*, at 326, quoting *Hansgirg v. Kemmer*, 40 U.S.P.Q. 665, 667 (C.C.P.A. 1939); *In re Rijckaert*, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993), quoting *Oelrich*, at 326; see also *Skinner*, at 1789. "Inherency ... may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Skinner*, at 1789, citing *Oelrich*. Where anticipation is found through inherency, the Office's burden of establishing prima facie anticipation includes the burden of providing "...some evidence

or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art." *Skinner* at 1789.

Claims 31, 32 and 38-54 stand rejected under35 U.S.C. §102(e) as allegedly being anticipated by ***Bunker.*** Applying the legal standards set forth above, it is respectfully submitted that the Examiner erred in rejecting independent claims 31, 38 and the claims depending therefrom. In the Advisory Office Action, the Examiner maintained the anticipation rejection of claims 31, 32 and 38-54 over ***Bunker***. Appellants first address the rejection of claim 31.

2. The disclosure of *Bunker*

Bunker notes that testing an Embedded DRAM 10 presents new problems not encountered when testing conventional DRAMs. Col. 2, lines 26-31. More specifically, an external memory tester must transfer test data to and from the memory cells in the DRAM 14. The memory tester must be coupled to the DRAM 14 through the external terminals 24 on the Embedded DRAM 10, and must apply address, control, and data signals on such external terminals to transfer data to and from the memory cells in the DRAM 14. Due to the wide internal data bus 20 of the DRAM 14, however, there are many fewer external terminals 24 available on the Embedded DRAM 10 than there are data lines in the internal data bus 20. For example, if the internal data bus 20 is 512 bits wide, the Embedded DRAM 10 cannot include 512 external data terminals plus address and control terminals due to the physical limitations of forming such external terminals

24. Thus, in an Embedded DRAM there is a problem in transferring data between the DRAM and the memory tester when testing the DRAM. Col. 2, lines 31-47.

To this end, ***Bunker*** is directed to utilizing ***parallel*** data compression ***circuits*** to ***simultaneously*** test Embedded DRAMs having ***wide internal data*** paths. More specifically, ***Bunker*** discloses a test circuit in an Embedded DRAM enables a memory tester to test the DRAM portion of the Embedded DRAM. Col. 2, lines 48-50. According to ***Bunker***, the test circuitry 206 is contained in the memory 210, and operates during a first test mode to compress test data read from a plurality of memory-cell arrays A_1 -A_8 and generate a plurality of error signals E1-E8 that are output to the memory tester 202. In response to one of the error signals E1-E8 going active, the test circuitry 206 thereafter operates in a second test mode during which it enables the memory tester 202 to determine the specific address of a defective memory-cell in one of the arrays A_1 -A_8. Col. 3, lines 44-53. The test circuitry 206 includes ***a plurality of data compression circuits*** DC1-DC8 246a-246h, each of the data compression circuits receiving the same bit from each of the data masking circuits DM1-DM8. Col. 5, lines 23-26. Each of the data compression circuits DC1-DC8 determines whether each of the bits applied on its inputs has the same binary value, and generates a corresponding error signal E1-E8 in response to this determination. Col. 5, lines 32-35. In this way, ***Bunker*** compresses each data bit simultaneously with other data bits using a corresponding compression circuit to evaluate binary values in a parallel operation.

More specifically, when each of the applied read data bits has the same binary value, each of the data compression circuits DC1-DC8 drives its corresponding error

signal E1-E8 inactive, and when any of the applied read data bits applied to a given data compensation circuit DC1-DC8 has a binary value different from that of the other applied read data bits, the data compression circuit DC1-DC8 drives the corresponding error signal E1-E8 active. Col. 5, lines 38-45. The data compression circuits DC1-DC8 may include circuitry to compare each of the applied read data bits to a corresponding predetermined value. Col. 5, lines 54-57.

Bunker teaches that during the mask mode of operation, the test control circuit 246 ***sequentially activates the byte mask signals*** DQM0-DQM7 in order to enable the memory tester 202 to determine the specific memory cell that is defective. For example, in ***Bunker*** the data compression circuit DC8 drives the E8 signal active. Col. 6, lines 59-63. The data bit from the data masking circuit DM8 that is applied to the compression circuit DC8 is masked. When the **data bit from the masking circuit DM8 is *masked***, the compression circuit DC8 **compares** the binary values of the **bits from all other masking circuits** DC1-DC7 and generates the error signal E8 in response to this comparison. Col. 6, line 63- col. 7, line 5.

3. Claim 31 is allowable over *Bunker*

By way of the background, independent claim 31 generally requires masking the latched data from said at least two of a plurality of data lines. The masked data is compressed to determine if the masked data matches a predetermined pattern using a compressing circuit. This invention provides various advantages over the cited prior art. For example, as disclosed in the Appellants' Specification on page 12, lines 5-12, the memory device cores 110 share a compression circuit 125, thus permitting each of the

memory device cores 110 to be tested without duplicating compression logic. This is an exemplary advantage that is not present in the prior art.

Claim 31 is directed to a method for testing a memory device having a plurality of data lines. The method comprises masking the latched data from at least two of the plurality of data lines that are latched from two respective memory portions. The method further includes compressing the masked data to determine if the masked data matches a predetermined pattern using a compressing circuit. The method (1) masks the latched data from two respective memory portions and (2) uses a compressing circuit that compresses this masked data.

The Examiner alleges that ***Bunker*** teaches all the elements of claim 31. The Applicants respectfully disagree and assert that ***Bunker*** at least does not teach or suggest (1) masking the latched data from at least two of the plurality of data lines that are latched from two respective memory portions and (2) compressing the masked data to determine if the masked data matches a predetermined pattern using a compressing circuit.

The Examiner argues that the "memory portions" of claim 31 corresponds to the Arrays A1-A8 in ***Bunker***, and "a compressing circuit" with single compression logic shared across multiple memory cores corresponds to the "eight compression circuits DC1-DC8 each having its own compression logic, which is duplicated eight times to compress the stored data in eight corresponding data masking circuits" disclosed in ***Bunker***. *See* Final Office Action, p. 6. Applicants respectfully disagree. Instead, claim 31 generally requires masking the latched data from two respective memory portions (for

example, two memory cells of a single memory core and not two memory cells from two different arrays). This masked data may be compressed to determine if the masking of the latched data from two respective memory portions matches a predetermined pattern using a compressing circuit.

While ***Bunker*** teaches a mask mode of operation, in which the test control circuit 246 sequentially activates the byte mask signals DQM0-DQM7 in order to enable the memory tester 202 to determine the specific memory cell that is defective, but it is the same memory cell (for example, memory cell 1) across all the eight arrays A1-A8 rather than two respective memory portions (e.g., cells) of a single memory core. For example, in ***Bunker*** the data compression circuit DC8 drives the E8 signal active and the data bit from the data masking circuit DM8 that is applied to the compression circuit DC8 is masked. Col. 6, lines 59-63. When the data bit from the masking circuit DM8 is masked, the compression circuit DC8 compares the binary values of the bits from all other masking circuits DC1-DC7 each associated with a different array A1-A8 and generates the error signal E8 in response to this comparison. Col. 6, line 63- col. 7, line 5. Thus, the cited reference does not teach or suggest masking the latched data from two respective memory portions.

The Examiner further alleges that ***Bunker*** discloses "a composite compression circuit" comprising the sub-circuits DC1-DC8 in Figure is a shared device. *See*, the Final Office Action p. 6. This is plainly incorrect. A closer review of ***Bunker*** reveals that the so called sub-circuits DC1-DC8 ("composite compression circuit" according to the Examiner) are, in fact, compression logic duplicated eight times, which is, not a

compressing circuit (having single compression logic shared across respective memory portions), as called for by claim 1. See ***Bunker,*** Col. 5, lines 54-57 (stating the data compression circuits DC1-DC8 may include circuitry to compare each of the applied read data bits to a corresponding predetermined value).

As disclosed in the Applicants' Specification on page 12, lines 5-12, the memory device cores 110 share a compression circuit 125, thus permitting each of the memory device cores 110 to be tested without duplicating compression logic. The compression circuit 125 receives and compresses a plurality of the DQ lines 120 and provides an output indicating whether the data present on the DQ lines 120 that was read from one of the memory device cores 110 matches the pattern that was written into that memory device core 110. Unlike the compression circuit 10 of Figure 1, the compression circuit 125 compresses data on the DQ lines 120 leaving the memory device cores 110, as opposed to the I/O lines within the memory device cores 110. This allows sharing of the compression circuit 125 by the memory device cores 110 for testing thereof without duplicated compression logic. Accordingly, the reference cited by the Examiner do not teach the claimed feature of a compressing circuit for compressing the masked data from at least two of the plurality of data lines that are latched from two respective memory portions. Thus for this reason alone, claim 31 is allowable.

With the above understanding of ***Bunker*** and claim 31, it is respectfully submitted that the Examiner erred in several respects in rejecting independent claim 31. Claim 31 involves latching data present on at least a subset of the plurality of data lines **BASED UPON** an enable signal, masking the latched data from the at least two of the

plurality of data lines, and compressing the masked data to determine if the masked data matches a predetermined pattern using a compressing circuit. At no point does ***Bunker*** suggest such a methodology. The Examiner relies on the disclosure of Figure 2 as well as Col. 5, lines 58-67 and Col. 2, lines 50-53, in ***Bunker*** as support for disclosure of this limitation. Appellants respectfully disagree. All that Figure 2 of ***Bunker*** discloses is that, in response to a test mode signal TM and a plurality of control signals 248 from the memory tester 202, a test control circuit 246 of the test circuitry 206 generates a plurality of control signals 250 along with the byte-mask signals DQM0-DQM7. The plurality of control signals 250 and the byte-mask **(FIXED 8-bit)** signals DQM0-DQM7 control operation of the data masking circuits DM1-DM8, data compression circuits DC1-DC8. Col. 5, lines. 50-53. This disclosure does not anticipate.

Appellants respectfully assert that ***Bunker*** does not teach, disclose or suggest latching data present on at least a **subset** of the plurality of data lines **BASED UPON** an enable signal, **masking the latched data** from the at least two of the plurality of data lines, and **compressing the masked data** to determine if the masked data matches a predetermined pattern **using a compressing circuit**, as called for by claim 31. In asserting that this limitation is disclosed in ***Bunker***, the Examiner purports to draw an analogy between the teachings of ***Bunker*** and the claimed subject matter. See Final Office Action, pages 3-4. The Examiner's argument is flawed for several reasons. First, it is well established that to be an anticipatory reference under §102(e), the reference must disclose identically each and every claim element. An **objective** reading of ***Bunker*** leads to the inescapable conclusion that ***Bunker*** is simply not concerned with selectively mask out a subset of latched data lines for compressing using a single compression

circuit. Respectfully, any contention to the contrary is based upon an improper use of Appellants disclosure when viewing the disclosure of ***Bunker***. Accordingly, for this reason alone ***Bunker,*** fails to anticipate claim 31. However, there are additional reasons why ***Bunker*** does not anticipate all elements of claim 31.

Claim 31 also requires compressing the masked data to determine if the masked data matches a predetermined pattern using a compressing circuit. This methodology is simply not disclosed nor suggested in ***Bunker***. Instead of compressing the masked data using a compressing circuit, ***Bunker*** causes bit-by-bit masking in that the data masking circuit masks each data signal responsive to a data masking signal. Col. 8, lines 20-22. ***Bunker*** controls ***the data masking signals to sequentially mask respective data signals applied to the data compression circuits*** to enable an external tester to detect a defective memory cell from the generated error signals. Col. 8, lines 46-50. By sequentially activating each of the masking signals and causing the data masking circuit to drive the error signal inactive when the erroneous data signal is masked; the test control circuit detects a defective memory cell storing an erroneous data signal. Col. 8, lines 20-22.

Moreover, ***Bunker*** does not use a compressing circuit to compress the masked data from the at least two of the plurality of data lines. In the Final Office Action at page 5, the Examiner stated that the compression circuit of ***Bunker*** is a "circuit comprising the sub-circuits DC1-DC8 in Figure 2" since all of the sub-circuits DC1-DC8 are required and act as a unit to process all of the I/O lines from memory array (A1-A8) and disposed on the single embedded-memory semiconductor. Appellants respectfully disagree. That is, a sub-circuit with compression logic is duplicated eight times on a per I/O line basis to

provide a functionality of an 8-bit wide compression circuitry for each memory array. In other words, the Examiner does not rely on any express disclosure in ***Bunker*** to teach use of a compression circuit for compressing the masked data from at least two of the plurality of data lines. Instead, the Examiner merely makes a conclusionary statement to this effect. At most, the Examiner alleges that since ***Bunker*** individually or independently compresses all of the I/O lines, therefore, ***Bunker*** allegedly teaches compressing the masked data from at least two of the plurality of data lines using a compression circuit. In this way, the Examiner simply concludes that individually or independently compresses data on all of the I/O lines is same as compressing the masked data from at least two of the plurality of data lines using a compression circuit. Appellants respectfully disagree.

The Examiner conspicuously fails to provide any support from ***Bunker*** as to precisely which "compression circuit" compresses the masked data from at least two of the plurality of data lines. Indeed, ***Bunker*** teaches that a sub-circuit of a compression circuit is used for each individual I/O line of a memory array. The Examiner cannot contend that this sub-circuit of a compression circuit is the "compression circuit" because the Examiner argues that this compression circuit corresponds to the "eight sub-circuits" recited as a single compression circuit in claim 31. In other words, the Examiner cannot use the sub-circuit of a compression circuit to satisfy the recited claimed feature of a single compression circuit. This is clearly improper. In the instant case, because the Examiner asserts that the eight sub-circuits correspond to the "compression circuit," the Examiner has failed to show which single "compression circuit" is used by the apparatus of ***Bunker*** reference to compress the masked data from at least two of the plurality of

data lines. For this reason, claim 31 is allowable.

While ***Bunker*** teaches individually or independently compressing I/O lines, the compression circuit is not used to compress the masked data from at least two of the plurality of data lines as required by claim 31. As described above, ***Bunker*** is simply not concerned with selectively compressing the masked data from a subset of the plurality of data lines. ***Bunker*** compresses data on all of the I/O lines using a compression logic that is duplicated eight times on a per I/O line basis. For at least the aforementioned reasons, it is respectfully submitted that claims 1 and claims dependent there from are not anticipated by the art of record.

Appellants respectfully further assert that in the Final Office Action dated October 5, 2005, the Examiner erred in interpreting the disclosure in ***Bunker***. In particular, for example, the Examiner asserted that since the abstract in ***Bunker*** explicitly teaches that each of the masked data signals from each of the activated buffers BUF1 - BUF8 in each of the Data Masking Circuits DMI-DM8 applied on its respective input is compared on to an expected value by the compression circuit DCI-DC8 in Figure 2 to produce a compressed error signal [E2,. . .,E8], ***Bunker*** compresses the masked data to determine if the masked data matches a predetermined pattern using a compressing circuit. Appellants respectfully disagree and respectfully assert that the Examiner misinterpreted the disclosure of Figure 2.

In ***Bunker,*** Figure 2 is a stylized illustration that provides a test circuitry 206, which includes the compression circuits DC1-DC8, 246a-246h, for convenience, the Figure itself merely illustrates DC8 and DC1. Perhaps this has caused some confusion as

to whether a compression circuit is respectfully corresponding to a memory array. However, the description in ***Bunker*** clarifies this issue. For example, the description in ***Bunker*** states that each of the data compression circuits DC1-DC8 receives a respective bit of read data applied on the data path from each of the arrays A1-A8. *See* column 5, lines 23-24. Thus, the Examiner has misinterpreted the use of the compression circuits and the memory arrays of Figure 2 to misapply the subject matter of ***Bunker*** to argue anticipation of the elements of claim 31 of the present invention. These arguments are described in further detail below.

The Examiner also states that "...the bottom line is the compression circuit comprising sub circuits DC1-DC8 in Figure 2, is still a compression circuit." This is a misapplication of the disclosure of ***Bunker***. Actually, what ***Bunker*** discloses is that the test circuitry 206 includes a plurality of data compression circuits DC1-DC8, 246A-246H. *See* column 5, lines 23-24. This is yet another example of the Examiner's misapplication of the disclosure of ***Bunker***. The Examiner is unable to point to any one compression circuit; instead the Examiner asserts that eight compression circuits DC1-DC8 of ***Bunker*** correspond to a compression circuit set forth in claim 31.

Additionally, in the Final Office Action dated October 5, 2005, the Examiner asserted that the Appellants' contention is "absurd". *See* second paragraph of page 6, of Final Office Action dated October 5, 2005. Appellants are saddened by this comment and respectfully disagree with the Examiner's characterization of Appellants' arguments.

Appellants have proven by citing disclosure in ***Bunker*** that the compression circuits, DC1-DC8, receive respective bit of read data applied to data compression circuit

from each of the arrays as called for by claim 1 of the present invention A1-A8. *See* column 5, lines 29-31. Simply because a data box may be shared does not mean that a memory array strictly only corresponds to a particular compression circuit. If the Examiner's logic were followed, then there would be no real need for eight compression circuits that somehow correspond to eight memory arrays. However, contrary to the Examiner's assertions, ***Bunker*** actually discloses eight compression circuits that correspond to eight memory arrays.

Additionally, the Examiner's attempt at grouping these into one large compression circuit is flawed since ***Bunker*** specifically cites in Figure 2, as well as in the Specification of ***Bunker***, that the test circuitry 206 includes a plurality of compression circuits DC1-DC8. *See* column 5, lines 23-24. Appellants respectfully assert that the Examiner's arguments are in error and that ***Bunker*** clearly does not disclose the compression circuit elements called for by claim 31 of the present invention. These arguments are further detailed below.

Regarding the element of latching data present on at least a subset of the plurality of data lines called for by claim 31 of the present invention, the Examiner has, again, misconstrued the disclosure of ***Bunker***. For example, the Examiner argued that the flip-flops HFF1-HFF8 and the buffers BUF1-BUF8 associated with each of the data masking circuits of ***Bunker*** are a plurality of data latches for use to matching data on a subset plurality of data lines. *See*, first paragraph of page 7 of the Final Office Action dated October 5, 2005. The Examiner had failed to consider that the element of claim 31 further recites that at least two of the plurality of data lines are latched from two

respective memory portions, the HFF and the buffers cited by the Examiner merely registers different data lines from the same memory portion, *i.e.*, from either array 1 or one of array 2 through array 8. In other words, ***Bunker*** does not disclose the latching of the data present on at least a subset of a plurality of data lines wherein at least two of the plurality of data lines are latched from two memory portions. ***Bunker*** merely latches data from any one of the memory portions or arrays A1-A8. Therefore, this is yet another claim element that is not taught, disclosed or suggested by ***Bunker***. These arguments are further detailed below.

In the Final Office Action dated October 5, 2005, regarding the element of compressing data to determine that the data matches a predetermined pattern as being anticipated, Appellants respectfully assert that the Examiner has again erred in interpreting the disclosure of ***Bunker***. For example, the Examiner cites the abstract, which recites that each data compression circuit compares each of the data signal applied to a respective input to an expected value and generates an active error signal. The Examiner uses this disclosure to read upon the matching of the predetermined pattern called for be claim 31. However, this passage in ***Bunker*** is further detailed and clarified as to how the error signals E1-E8 are generated. ***Bunker*** clearly describes that each of the data compression circuits, DC1-DC8, determines whether each of the bits applied on its inputs has the same binary value, and generates a corresponding error signal E1-E8 in response to this determination. *See* column 5 lines 32-35. Further, ***Bunker*** discloses that when each of the applied read data bits has the same binary value, each of the data compression circuits, DC1-DC8, drives its corresponding error signal E1-E8 inactive...". *See* column 5, lines 38-41. Therefore, the Examiner is in error as to how the error signals

E1-E8 are generated. Rather than determining whether the mass data matches a predetermined pattern, ***Bunker*** is directed to determining whether each of the bits applied to the inputs of the compression circuits has the same binary value.

The data compression circuits, which includes circuitry to compare each of the applied read bits to a corresponding predetermined value disclosure in ***Bunker***, is not sufficient enabling disclosure to anticipate all of the elements of claims 31 and 38 of the present invention. As described in further details below, simply disclosing that the data compression circuits may include circuitry to compare each of the applied read bits does not disclose or anticipate compressing the data to determine if the data matches a predetermined pattern. As described herein, ***Bunker*** does not disclose latching data present on a subset of a plurality of lines in latch form to respective memory portions and masking the data and compressing the masked data to determine whether it matches a predetermined pattern, as called for by claims 31 and 38 of the present invention. ***Bunker*** merely masks data using separate data masking circuitry DM1-DM8 that correspond to array A1-A8. Therefore, ***Bunker*** does not mask data lines from at least a subset of a plurality of data lines from two respective memory portions. Therefore, ***Bunker*** couldn't possibly disclose compressing the masked data and comparing it to a predetermined pattern. These arguments are further detailed below.

As described above, claim 31 calls for latching a plurality of data lines, wherein two data lines are latched from two respective memory portions. Claim 31 also calls for masking the latched data lines and compressing the masked data lines using a compression circuit. Therefore, claim 31 calls for compressing latched data lines where

at least two of the data lines from two different memory portions are compressed by a compressing unit. In contrast to claim 31, ***Bunker*** discloses a system where each memory array (A1-A8) corresponds with a particular data compression circuit (DC1-DC8). In other words, ***Bunker*** discloses that data from each memory array must be compressed by a separate, corresponding compression circuit. *See*, Figure 2, column 5, lines 23-35. In contrast to ***Bunker***, claim 31 recites a method that calls for a compressing circuit to compress data from at least two memory portions. Various advantages provided by the method in claim 31 is described in the specification, which includes but is not limited to, allowing a compression to be shared by a plurality of memory portion, *e.g.*, memory core, allowing for ease of re-design of memory, e.g., increasing memory density without adding additional compressing circuit. *See* for example, page 12, lines 5-15 of the Specification. These advantages would not be available in the system disclosed in ***Bunker***.

The system in ***Bunker*** clearly describes that each memory portion requires a corresponding compression circuit. This disclosure does not anticipate or make obvious the method recited in claim 31, which calls for a compressing circuit to compress data from at least two memory portions. Therefore, for at least this reason, all of the elements of claim 31 are not anticipated or made obvious by ***Bunker***. Additionally, independent claim 38 calls for means for masking the latched data lines and means for compressing the masked data lines using a compression circuit. For at least the reasons cited above, claim 38 is also not anticipated by ***Bunker*** since ***Bunker*** requires that each memory portion be associated with a corresponding compressing/compression circuit. Therefore, claim 38 is also allowable for at least the reasons cited above.

There are additional reasons that support Appellants' assertions that claims 31 and 38 of the present invention are allowable over ***Bunker***. For example, ***Bunker*** discloses a plurality of data masking circuits, DM1, DM2, that are coupled to particular arrays, A1 and A2. *See*, Figure 2, column 4, lines 14-19. The masking function disclosed by ***Bunker*** merely receives an array of data for each masking circuit, wherein one or more of the data lines called for by claim 31 of the present invention, is masked based upon an enable signal. Therefore, the disclosure of ***Bunker*** does not read upon all of the elements of claim 31.

Further, the function performed by the compression circuits DC1-DC8 disclosed by ***Bunker*** all receive a respective bit of read data that is applied on the data above from each of the arrays A1-A8. *See*, column 5, lines 29-31. The compression circuits DC1-DC8 make a determination whether each of the bits applied upon its inputs has the same binary value and generates an error signal E1-E8 in response. *See,* column 5, lines 31-35. ***Bunker*** discloses that if any of the applied read data bits applied to the compensation compression circuit DC1-DC8, has a binary value different from that of the other applied data bits, the error signal is generated. In contrast to ***Bunker***, the compression circuit called for by claim 31 of the present invention calls for detecting a predetermined pattern on a subset of data lines and to provide a pass signal when the predetermined pattern is detected on the subset of data lines. Therefore, ***Bunker*** does not disclose performing the detection of the predetermined pattern, as called for by claim 1 of the present invention.

Bunker merely discloses comparing the binary value of the bits of the compensation circuit DC1-DC8 to determine whether they are equal in value, therefore,

the predetermined pattern detection is not performed or disclosed by ***Bunker***. Hence, another aspect of the elements of claim 1 are not disclosed, taught, or suggested by ***Bunker***. ***Bunker*** discloses that in the masking mode, which is the mode used to read upon the claims of the present invention, when the data bit from the masking circuit is masked, the compression circuit compares the binary value of the bits from all other masking circuits and generates an error signal in response to this comparison. This is performed for individual masking circuitry and compression circuits. *See,* column 7, lines 2-6. It is clear that the system of ***Bunker*** discloses comparing binary values from other masking circuits by the compression circuit to generate an error signal. In contrast, claim 31 calls for detecting a predetermined pattern on a subset of data lines to determine whether a pass signal is to be provided based upon comparison to a predetermined pattern. This is not taught, disclosed, or suggested by ***Bunker***, which relies on comparing binary values of each bit applied to the inputs of the compression circuits DC1-DC8 to determine that an error signal is asserted. Therefore, ***Bunker*** does not disclose, teach, or suggest, all of the elements of claim 1 of the present invention.

In contrast to ***Bunker***, claim 31 calls for compressing the masked data to determine if the masked data actually matches a predetermined pattern. ***Bunker*** discloses that the test circuitry operates during a first test mode to compress test data from a plurality of memory cell arrays to generate an error signal. ***Bunker*** does not disclose compressing mask data if the mask data matches a predetermined pattern. ***Bunker*** discloses that data compression circuits include circuitry to compare each of the read data bits to see if it has a binary value different from that of other applied read data bits.

However, ***Bunker*** does not disclose compressing the masked data to determine if the mask data matches a predetermined pattern.

The Examiner cites column 5, lines 54-57 in ***Bunker*** to assert that it teaches that the masked data is compressed within the compression circuits DC1-DC8 by comparing each of the applied read mask bits to a predetermined value to determine if the applied read matches the predetermined value. However, Appellants respectfully assert that column 5, lines 54-57, discloses that the data compression circuits may include circuitry to compare each of the applied read data bits to a corresponding predetermined value, which may then be used to generate an error signal. However, ***Bunker*** does not disclose compressing the mask data to determine if the mask data matches the predetermined pattern. ***Bunker*** provides data into different arrays A1-A8 into the masking circuit. In contrast, claim 31 calls for latching data present on a subset of plurality of data lines and masking the data, wherein each masking circuit is provided an array of data according to ***Bunker***, which is not taught or suggested by ***Bunker***. Furthermore, claim 31 calls for compressing the masked data to determine if the masked data matches the predetermined pattern to provide a pass signal if there is a match. ***Bunker*** does not disclose compressing the masked data to determine if the masked data matches a predetermined pattern. ***Bunker*** merely discloses that the data compression circuit examines whether the binary value of a read bit is different from that of another read bit.

Appellants have demonstrated that several elements of claim 31 are not taught, disclosed, or suggested by ***Bunker.*** Accordingly, the Examiner erred in rejecting claim

31 and hence, all of the elements of claim 31 are not disclosed, taught, or suggested by ***Bunker***.

Additionally, claim 38 provides for a means plus function apparatus claim that calls for means for performing the similar function(s) described previously. In particular, claim 38 includes means for masking the latched data from the at least two of the plurality of data lines, wherein at least two of the plurality of data lines are latched from two respective memory portions. Claim 38 further includes means for compressing the masked data to determine if the data matches a predetermined pattern using a compressing circuit and means for providing at least a pass signal if the data matches the predetermined pattern. ***Bunker*** is directed to a test circuitry that operates during a first test mode to compress test data from a plurality of memory cell arrays to generate an error signal. ***Bunker*** discloses compressing an unmasked bit, wherein claim 38 calls for means for compressing the masked data. ***Bunker*** generates an error signal from testing a corresponding memory cell across a plurality of memory arrays instead of providing a pass signal if the masked data latched from two respective memory portions matches a predetermined pattern. For aforementioned reasons, claim 38 is not taught, disclosed, or suggested by ***Bunker***. Therefore, claim 38 is also allowable for at least the reasons cited above.

Further the method of dependent claim 45 comprises providing a plurality of latches for latching the data associated with the subset, receiving a clock signal and a latch signal, and latching the data based on a first combination of the latch signal and the clock signal. ***Bunker*** discloses storing the data and uses a byte masking signal or bit

registers, wherein claim 38 calls for latching the data based on a first combination of the latch signal and the clock signal. For aforementioned reasons, claim 45 is not taught, disclosed, or suggested by ***Bunker***.

Appellants respectfully request the rejections of claims 31-32 and 38-54 over ***Bunker*** be REVERSED because the prior art does not teach or suggest any of the pending claims.

C. Claims 31, 32 and 38-54 Are Allowable Over *Bunker*

The Examiner rejected claims 31, 32 and 38-54 under 35 U.S.C. 102(f) asserting that the Appellants did not invent the claimed subject matter in view of U.S. Patent No. 6,311,299 (***Bunker***)". Appellants respectfully traverse this rejection.

As described above, independent claims 31 and 38 refer to compressing latched data lines where at least two of the data lines from two different memory portions are compressed by a compressing unit. These elements are not taught, disclosed, or suggested by ***Bunker***. Therefore, ***Bunker*** could not be prior art to claims of the present invention. Hence, Appellants respectfully assert that Examiner's assertion that Appellants did not invent the claimed subject matter is incorrect.

Additionally, as described above, ***Bunker*** does not disclose all of the elements of claims 31 and 38; for example, ***Bunker*** does not disclose compressing the masked data to determine if the masked data matches a predetermined pattern. Claim 31 calls for compressing the masked data to determine if the masked data matches a predetermined pattern, wherein ***Bunker*** is directed to a test circuitry that operates during a first test

mode to compress test data from a plurality of memory cell arrays to generate an error signal. Further, ***Bunker*** discloses compressing an unmasked bit, wherein claims 31 and 38 call for compressing a masked bit, which is yet another example of the reasons why ***Bunker*** does not anticipate claims 31 and 38 of the present invention. Other examples of the reasons why ***Bunker*** does not disclose all of the elements of claims 31 and 38 are provided above in the previous section. Therefore, claims 31 and 38 are allowable for at least the reasons cited above.

Appellants respectfully request the rejections of claims 31-32 and 38-54 over ***Bunker*** be REVERSED because the prior art does not teach or suggest any of the pending claims.

VIII. CLAIMS APPENDIX

The claims currently under consideration, *i.e.,* claims 31, 32 and 38-54, are listed in the Claims Appendix attached hereto.

VII. EVIDENCE APPENDIX

There is no evidence relied upon in this Appeal with respect to this section.

VIII. RELATED PROCEEDINGS APPENDIX

There are no related appeals and/or interferences that might affect the outcome of this proceeding.

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims (claims 31, 32 and 38-54) pending in the present application over

the prior art of record. The undersigned attorney may be contacted at (713) 934-4069 with respect to any questions, comments, or suggestions relating to this appeal.

Respectfully submitted,
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CLAIMS APPENDIX

1-30 (Cancelled)

31. (Previously Amended) A method for testing a memory device having a plurality of data lines, comprising:

latching data present on at least a subset of the plurality of data lines based upon an enable signal, wherein at least two of said plurality of data lines are latched from two respective memory portions;

masking the latched data from said at least two of said plurality of data lines;

compressing the masked data to determine if the masked data matches a predetermined pattern using a compressing circuit; and

providing at least a pass signal if the masked data matches the predetermined pattern.

32. (Previously Amended) The method of claim 31, wherein compressing the masked data further comprises determining if each datum of the data matches a predetermined value.

33-37 (Cancelled)

38. (Previously Amended) An apparatus for testing a memory device having a plurality of data lines, comprising:

means for latching data present on at least a subset of the plurality of data lines based upon an enable signal, wherein at least two of said plurality of data lines are latched from two respective memory portions;

means for masking the latched data from said at least two of said plurality of data lines;

means for compressing the masked data to determine if the data matches a predetermined pattern using a compressing circuit; and

means for providing at least a pass signal if the data matches the predetermined pattern.

39. (Previously Presented) The method of claim 31, further comprising:

providing a plurality of latches for latching the data associated with the subset;

providing a plurality of enable signals to the latches; and

disabling latches in the plurality of latches responsive to a deassertion of the associated enable signals.

40. (Previously Presented) The method of claim 39, wherein disabling the latches further comprises forcing the disabled latches to output a predetermined voltage.

41. (Previously Presented) The method of claim 40, wherein forcing the disabled latches to output the predetermined voltage further comprises forcing the disabled latches to output a voltage corresponding to a logic 1.

42. (Previously Presented) The method of claim 40, wherein forcing the disabled latches to output the predetermined voltage further comprises forcing the disabled latches to output a voltage corresponding to a logic 0.

43. (Previously Presented) The method of claim 39, further comprising:

receiving a latch signal; and

latching the data responsive to the latch signal being asserted in the latches with associated enable signals asserted.

44. (Previously Presented) The method of claim 43, further comprising bypassing the latch responsive to the latch signal being deasserted.

45. (Previously Presented) The method of claim 31, further comprising:

providing a plurality of latches for latching the data associated with the subset;

receiving a clock signal and a latch signal; and

latching the data based on a first combination of the latch signal and the clock signal.

46. (Previously Presented) The method of claim 31, wherein compressing the masked data further comprises performing a NAND Boolean function.

47. (Previously Presented) The method of claim 31, wherein compressing the masked data further comprises performing a NOR Boolean function.

48. (Previously Presented) The apparatus of claim 38, wherein the means for masking the latched data further comprises means for disabling the latching means responsive to deassertions of enable signals associated with the data lines in the subset.

49. (Previously Presented) The apparatus of claim 48, wherein the means for disabling further comprises means for forcing the disabled latches to output a predetermined voltage.

50. (Previously Presented) The apparatus of claim 49, wherein the predetermined voltage corresponds to a logic 1.

51. (Previously Presented) The apparatus of claim 49, wherein the predetermined voltage corresponds to a logic 0.

52. (Previously Presented) The apparatus of claim 38, further comprising means for bypassing the latching means responsive to a deassertion of a latch signal.

53. (Previously Presented) The apparatus of claim 38, wherein the means for compressing the masked data further comprises means for performing a NAND Boolean function.

54. (Previously Presented) The apparatus of claim 38, wherein the means for compressing the masked data further comprises means for performing a NOR Boolean function.